REMARKS

Applicant has amended claims 8, 10-13, 18-22 and added new claim 23. No new matter has been added by these amendments as can be confirmed by the Examiner. Claims 1-23 remain in the application. Applicant respectfully requests reconsideration of the objections and the rejections set forth in the Office Action dated November 2, 2005.

Claim Objections

Claims 10-13 and 18-22 were objected to under 37 CFR 1.75(c) as being of improper dependent form for failing to further limit the subject matter of a previous claim.

Applicant has amended the preamble of claims 10-13 to read "The method of claim 9." Applicant submits that claims 10-13, as amended, further limit the subject matter of claim 9, and therefore overcome the objection.

Applicant has amended the preamble of claims 18-22 to read "The method of claim 17." Applicant submits that claims 18-22, as amended, further limit the subject matter of claim 17, and therefore overcome the objection.

Claim Rejections under 35 U.S.C. § 102

Claims 1-22 were rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Hoare et al. (U.S. Patent Application Publication 20020133325). Applicant respectfully traverses.

Regarding independent claim 1, Hoare fails to disclose, teach or suggest "at least one macro processor programmed into said programmable logic device." (emphasis added). A macro processor is a processor capable of executing macro-level

instructions, e.g., "multiply", "multiplex" etc. The macros of Hoare simply refer to groups of primitive logic gates joined as macros and in no way disclose, teach or suggest macro processors (Hoare, paragraph [0084]). The "macro block (logic) engine" relied upon by the Examiner actually refers to the simulation engine used to simulate the primitives and macros and is not itself programmed into a programmable logic device as required by independent claim 1. In fact, Hoare only teaches mapping a gate level design into a Programmable Logic Device (PLD) (Hoare, paragraph [0080]). Hoare makes no mention of programming any type of processor into a programmable logic device, much less a macro processor. Thus, Hoare fails to disclose, teach or suggest a macro processor programmed into a programmable logic device as required by independent claim 1. Consequently, Hoare also fails to disclose, teach or suggest "said at least one macro processor utilizing at least one of said plurality of logic elements of said programmable logic device, said at least one macro processor comprising a macro functional unit that executes macro instructions."

For these reasons, Applicant submits that claim 1 is patentable and respectfully requests that the rejection of claim 1 be withdrawn.

Claims 2-7 depend from claim 1, and are therefore patentable for at least the reasons given for claim 1.

Independent claim 8 has been amended to make clear that "said processor types" are programmed "into said at least one programmable logic device." Hoare fails to disclose, teach or suggest "mapping the user design into operations for execution; partitioning each of said operations into processor types suitable for each of said operations" and "programming said processor types into said at least one programmable logic device." (emphasis added). In contrast, Hoare explicitly teaches gate level simulation, in which the user design is transformed into a gate level design, instead of processor types, and the gate level design is mapped into the programmable

logic device (Hoare, paragraphs [0079-0081]). The gate level simulation of Hoare is not remotely the same as partitioning the operations of a user design into processor types and programming the processor types into a programmable logic device as required by independent claim 8.

Consequently, the portions of Hoare relied upon by the Examiner fail to disclose, teach or suggest the claim limitations of claim 8. For example, paragraphs [0080] and [0102] fail to disclose, teach or suggest programming the processor types into a programmable logic device. Paragraph [0080] explicitly teaches mapping gate level designs into programmable logic devices instead of processor types and paragraph [0102] makes no mention of programming processor types into a programmable logic device. The simulation engines in paragraph [0067] relied upon by the Examiner as teaching the processor types actually refer to the simulation engines that perform the circuit simulation, and are not themselves programmed into a programmable logic device.

By partitioning the operations of a user design into processor types and programming the processor types into a programmable logic device, the verification system of claim 8 avoids the need to implement logic, as in Hoare's gate level simulation, and also avoids the need to compile the design to be verified into many gate-level Boolean logic operations for logic processors as in existing processor based acceleration and emulation systems. This results in improved efficiency in the form of lower cost, lower power and/or higher speed when verifying certain types of designs.

For these reasons, Applicant submits that independent claim 8 is patentable over Hoare, and respectfully requests that the rejection of claim 8 be withdrawn.

Claims 9-16 depend from claim 8, and are therefore patentable for at least the reasons given for claim 8. Dependent claim 9 is additionally patentable because Hoare fails to disclose, teach or suggest programming logic processors, macro processors,

memory processors and general purpose processors into a programmable logic device. The portion of Hoare relied upon by the Examiner (paragraph [0031]) does not mention any processor, much less the processors recited in dependent claim 9.

Independent claim 17 requires a macro processor programmed into a programmable device, and is therefore patentable for the same reasons give for claim 1.

Claims 18-22 depend from claim 17, and are therefore patentable for at least the reasons given for claim 17.

New Claim

New claim 23 depends from claim 1, and is therefore patentable for the reasons given for claim 1. New claim 23 is additionally patentable because Hoare fails to disclose, teach or suggest a macro processor programmed into a Field Programmable Gate Array.

Conclusion

For at least the reasons set forth above, it is submitted that claims 1-23 are in condition for allowance. A Notice of Allowance is earnestly solicited. The Examiner is encouraged to contact the undersigned at (949) 567-6700 if there is any way to expedite the prosecution of the present application.

Respectfully submitted,

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